IN THE CLAIMS:

Please amend the claims as follows:

1. (currently amended) A semiconductor test apparatus comprising:

a first time interpolator which receives a clock output from a device under test, obtains the clock by using a plurality of strobes having specified timing intervals, outputs ~~it~~ the obtained clock as time-series level data, selectively receives level data indicative of an edge timing of a rise edge and/or a fall edge of the level data, and outputs positional data indicative of an edge timing of the selected level data;

a second time interpolator which receives output data output from the device under test, obtains the output data by using a plurality of strobes having specified timing intervals, and outputs ~~it~~ the obtained output data as time-series level data;

a digital filter which receives and holds the positional data output from the first time interpolator, and outputs a recovery clock indicative of a predetermined edge timing from one or more sets of the positional data; and

a data selection circuit which receives the time-series level data output from the second time interpolator, selects the level data with an edge timing of the recovery clock

output from the digital filter, and outputs ~~it~~ the selected level data as measurement data of the device under test.

2. (currently amended) The semiconductor test apparatus according to claim 1, wherein:

the first time interpolator comprises a plurality of sequence circuits which receive clocks output from the device under test and are connected with each other in parallel; a delay circuit which sequentially inputs strobes delayed at specified timing intervals to the plurality of sequence circuits, and outputs time-series level data from the sequence circuits; an edge selector which selectively outputs level data indicative of a rise edge, level data indicative of a fall edge or level data indicative of the rise edge and the fall edge of the time-series level data output from the plurality of sequence circuits; and an encoder which receives level data selected by the edge selector, encodes ~~it~~ the selected level data into positional data indicative of an edge timing, and outputs ~~it~~ the positional data,

the digital filter comprises one or more registers connected with each other in serial which sequentially store the positional data output from the first time interpolator and output the stored positional data with a predetermined timing, and outputs a recovery clock indicative of a

predetermined edge timing from one or more sets of the positional data output from the registers,

the second time interpolator comprises a plurality of sequence circuits connected with each other in parallel which receive output data output from the device under test; and a delay circuit which sequentially inputs strobes delayed at specified timing intervals to the plurality of sequence circuits and outputs time-series level data from the sequence circuits, and

the data selection circuit comprises a selector which selects one set of data from the time-series level data input from the second time interpolator with the recovery clock output from the digital filter being used as a selection signal and outputs ~~it~~ the selected level data as measurement data of the device under test.

3. (original) The semiconductor test apparatus according to claim 2, wherein the edge selector comprises one or more selector circuits each of which comprises: a first AND circuit which receives a reverse output of one sequence circuit and a non-reverse output of a sequence circuit on a next stage; a second AND circuit which receives a non-reverse output of one sequence circuit and a reverse output of a sequence circuit on a next stage; an OR circuit which receives outputs of the first and second AND circuits; and a selector which selects one of outputs

of the first AND circuit, the second AND circuit and the OR circuit.

4. (previously amended) The semiconductor test apparatus according to claim 2, wherein the digital filter comprises an edge detection circuit which detects presence/absence of an edge of the positional data input from the first time interpolator and outputs the positional data stored in the register when the edge is detected.

5. (previously amended) The semiconductor test apparatus according to claim 4, wherein the register of the digital filter outputs the stored positional data with a predetermined timing irrespective of presence/absence of an edge of the positional data detected by the edge detection circuit.

6. (previously amended) The semiconductor test apparatus according to claim 2, wherein, when the two or more registers are provided, the digital filter comprises an average value calculation circuit which receives the positional data output from each of the two or more registers, calculates an average value of edge timings indicated by respective sets of the positional data, and outputs the average value as a recovery clock.

7. (currently amended) The semiconductor test apparatus according to claim 6, wherein the digital filter comprises an average value changeover switch which selects one of the positional data output from one register among the two or more

registers and the average value output from the average value calculation circuit and outputs ~~it~~ the selected output as a recovery clock.

8. (currently amended) The semiconductor test apparatus according to claim 2, wherein the digital filter comprises a timing correction circuit which adds a predetermined correction value to the positional data output from the register, corrects an edge timing indicated by the positional data and outputs ~~it~~ the corrected edge timing as a recovery clock.

9. (previously amended) The semiconductor test apparatus according to claim 1, further comprising a jitter detection circuit which receives a plurality of recovery clocks output from the digital filter, detects a phase difference between edge timings indicated by the respective recovery clocks and obtains a jitter of the clock of the device under test.

10. (previously amended) The semiconductor test apparatus according to claim 1, further comprising a bus which connects the first and second time interpolators with each other and distributes data output from the first and second time interpolators to a predetermined data selection circuit.